REMARKS

Section A of these Remarks responds to the 35 USC 102 rejections of the Office Action of March 12, while Section B responds to the 35 USC 103 rejections of that Action.

A. Claims 9, 12-15, 20-21, 24, 26, 27, 30-31, and 34; 102(e) Rejection: Discussion

Claims 9, 12-15, 20-21, 24, 26, 27, 30-31 and 34 are rejected under 35 USC 102(e) as being anticipated by Luoh et al, US Publication No. 2003/0017670.

This section begins with a response to the rejection of claim 9. Section A.1 describes evidence submitted in support of this response, Exhibits A-E. Section A.2 describes the difference between SONOS and floating gate devices. Section A.3 includes responses to the remaining 102 claim rejections.

Claim 9 recites a method for making a *SONOS device*, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer, *wherein the device is a SONOS device.*

Referring to FIG. 2 of Luoh et al., which pictures a floating gate memory device, not a SONOS device, the Examiner asserts:

> ... Luoh discloses a method for making a SONOS device, comprising: providing a channel region (area between source and drain 19 [0019]), and providing a first oxide layer 13 on the channel region by ISSG process providing a nitride layer 14, on the first oxide layer 13, and providing a second oxide layer 16 on the nitride layer [0020], wherein the device is a SONOS[sic].

The claim states, in both the preamble and the body, that the device is a *SONOS device.*

In a prior response, Applicants made the following argument: The claim includes the limitation that the device is a SONOS device. The device of Luoh et al. is a floating gate device, not a SONOS device, and thus the claim distinguishes over the device of Luoh et al. This

argument still applies. The Examiner responds to this argument in paragraph 7 of the March 12 Action:

> ... it is noted that the feature upon which the Applicant relies, i.e. SONOS layers are being contiguous layers are [sic] not recited in the rejected claim. Although the claim are [sic] interpreted in light of the specification, limitation from the specification are not read into the claim, see *In re Van Geuns* ... Furthermore, it is proper to use the specification to interpret what the applicant meant by a word or phrase recited in the claim. However, it is not proper to read the limitations appearing in the specification into the claim when these limitations are not recited in the claim.

Applicants believe the Examiner to be suggesting that because the term "SONOS device" is used in a claim without being fully defined in the claim, its meaning is uncertain. Applicants respectfully refute this point. Applicants reiterate that the term "SONOS device" is not of Applicants' own devising, nor does it require the description provided in the specification to define it. In this instance the author of the specification has not been "his own lexicographer"; on the contrary, the term "SONOS device" is a well-known term of art with an established and unambiguous meaning. The Examiner need not look to the present application for a description of a SONOS device (though such an explanation is provided); examples abound in trade and patent literature, and no limitations need be read into the claim from the specification to provide this meaning.

A.1 Exhibits A-E

As evidence, Applicants submit exhibits A-E, all examples of literature using the term "SONOS" or "SONOS device" to describe a field effect transistor which stores charge in a dielectric layer (typically a nitride layer), *not* in a conductive floating gate, as in the floating gate device of Luoh et al.

Exhibit A is a paper by She et al. titled "Silicon-Nitride as a Tunnel Dielectric for Improved SONOS-Type Flash Memory," which appeared in IEEE Electron Device Letters, Vol.

24, No. 5, in May 2003. The manuscript was received in January 2003, less than a year after the present application was filed. The paper begins: "The SONOS ... memory device has received a lot of attention due to its advantages *over the traditional floating-gate flash EEPROM device.*" (emphasis added), additional evidence supporting Applicants' contention that SONOS and floating gate devices are well-known and distinct. Fig. 1 of She et al. shows a SONOS device including the conventional SONOS layers with the variation that the usual tunneling oxide layer is replaced with a nitride layer, labeled "tunnel nitride", which innovation is the subject of the paper. It will be noted that the Index Terms, the well-known terms used to search for related topics listed immediately under the abstract, include "SONOS".

Exhibit B is a paper by Wu et al. titled "Impact of Nitride Process Conditions on SONOS Flash Devices," Journal of CCIT Vol. 32, No. 1, Nov. 2003; the manuscript was first received October 6, 2002, eight months after filing of the present application. Fig. 1 of Wu et al. again shows a typical SONOS device, showing the ONO stack (here labeled "Tunnel Oxide", "Silicon Nitride", and "Block Oxide") between a control gate and a substrate (here labeled P- Substrate), both of which are conventionally silicon. The first paragraph of the introduction includes the following sentence:

"In one promising structure, SONOS, the silicon nitride thin film as a replacement of conventional floating gate has been adopted ..."

Applicants believe this is further evidence that SONOS and floating gate memory devices are well known and distinct.

Exhibit C is an article from the website of Royal Philips Electronics of the Netherlands. Applicants regret that web formatting causes the right side of the text to be cut off. On the second page appears the heading "SONOS memories", under which appears the following text:

> "SONOS, which stands for Semiconductor-Oxide-Nitride-Oxide-Semiconductor, is a memory concept which was invented as long ago as the 1960's, but the concept was abandoned in the 1980's because of technological issues. Nowadays, these technological barriers have been overcome to a great extend, catalysed by the improved semiconductor fabrication methods. This has led to a revival of interest for SONOS devices, mainly driven by the better scaling perspectives and the ease of integration in a base line CMOS process, *compared to standard floating gate memories*. Moreover, some performance parameters, such as the write/erase endurance and the required programming voltages, exceed those of flash memories.
>
> Figure 3 shows a cross sectional view of a SONOS memory cell, made with a transmission electron microscope. Essentially, the cell is a conventional NMOS transistor, but with a gate dielectric consisting of a thermal oxide layer of approximately 2 nm thickness, a silicon nitride layer of about 5 nm and a second oxide layer with a thickness between 5 and 10 nm. At a positive gate bias, electrons can tunnel from the substrate through the ultra-thin oxide layer to the nitride layer, where they are subsequently trapped (silicon nitride has the intrinsic property to trap electrons). Due to this trapped negative charge, the threshold voltage of the transistor increases. Likewise, the threshold voltage can be decreased with a negative voltage on the gate, expelling the electrons from the nitride layer. So, roughly speaking, *the nitride layer takes over the role of the floating gate* in a standard flash cell."

Emphasis was added to show the distinction being made by the author between SONOS and floating gate cells.

Exhibit D is Bu et al, "Design Considerations in Scaled SONOS Nonvolatile Memory Devices". Fig. 1 of this paper contrasts the conventional floating gate and SONOS structures. The first paragraph of the Introduction includes the following sentence: "Two basic types of EEPROMs exist, namely, the floating gate device and the floating trap device, i.e. SONOS [3-4]." Applicants further point to the References section of this paper: references 1, 4, 13, 17, 19, 25, 27, 29, 31, and 33 use the term "SONOS" in the title, while references 2, 9, 10, 11, 14, 16, 24, 26, and 32 use the terms "MONOS" or "MNOS", which are variations, further evidence that the terms are well known.

Exhibit E is an excerpt from Volume 28 of *Cx-News*, a semiconductor technical information online publication from Sony Electronics (http://www.sony.net/Products/SC-

HP/cx_news/vol28/pdf/monos.pdf). In the second paragraph, this article gives an example of the terms "SONOS", "MONOS" and "floating gate" as used in the art:

> Figure 1 compares the MONOS and floating gate device structures. As can be seen in Figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data.

The MONOS device shown in Figure 1 of the Sony publication and the SONOS device of Fig. 1 of the present application both show a silicon channel, and, on the channel and in contiguous contact, an oxide layer, a nitride layer, a second oxide layer, and a gate conductor. In the SONY publication the gate conductor is metal, and in the present application it may be silicon. The Sony publication notes both the metal (MONOS) and silicon (SONOS) gate conductor variations. Similarly, the present application notes that the SONOS gate conductor is "typically of polysilicon, metal, or a silicide" (paragraph [19].)

It will be seen that the floating gate device pictured in Figure 1 of the Sony publication is essentially the same as the floating gate device in Fig. 2 of Luoh et al. In both, there is a channel, then on the channel and in contiguous contact, an oxide, a polysilicon floating gate, a dielectric layer, and a control gate. The difference lies in the dielectric between the floating gate and the control gate: In the Sony publication, this dielectric layer is a single layer of silicon dioxide, while in Fig. 2 of Luoh, the dielectric comprises layers 13-16, which are oxide, nitride, oxynitride, and oxide layers respectively, all dielectrics. As noted in paragraph [0004] of the Description of Prior Art in Luoh et al.:

> In conventional stacked non-volatile semiconductor memory devices, an insulating layer for insulating a floating gate and a control gate from each other is a single layer of silicon dioxide ...

In Luoh et al., the oxide-nitride-oxynitride-oxide stack is developed to provide better insulation between the floating gate 12 and the control gate 17, as the Description of Prior Art makes clear.

To summarize the evidence from Exhibits A-E, the term "SONOS device" is a well-known term of art, and its use has meaning without any need to read limitations into the claim from the specification. An apt analogy would be a claim describing a device as, for example, a "screwdriver" without actually including a definition of the term "screwdriver" in the claim. The term "screwdriver" is sufficiently well-known, as is the term "SONOS device" to those skilled in the art, to require no further definition in order to have a clear and well-understood meaning.

A.2 Description of SONOS and Floating Gate Devices

For clarity, Applicants repeat a summary of SONOS and floating gate devices provided in an earlier response:

Semiconductor nonvolatile memory devices that operate by storing charge fall largely into two categories: floating gate and SONOS.

SONOS is a well-known term of art. In a SONOS device, which typically operates as a memory cell, an oxide-nitride-oxide (ONO) dielectric structure separates a gate conductor, usually of silicon, from a channel, also usually of silicon. The sequence of contiguous layers, silicon-oxide-nitride-oxide-silicon, gives the SONOS device its name. The term MONOS is also used to describe a variation on these devices, in which metal replaces silicon in the gate conductor. An example of a SONOS device appears in FIG. 1 of the present application. Oxide layer 25, formed by ISSG, is a tunnel oxide. Charge is stored in nitride layer 35.

In contrast, in a floating gate device, as in FIG. 2 of Luoh et al., charge is stored not in a nitride later, but in an electrically isolated or "floating" conductive gate, normally of silicon. The device pictured in FIG. 1 of Luoh et al. is a floating gate device, containing floating gate 12.

A.3 Remaining claims: Discussion

Claims 12-15 all depend from claim 9, and thus include the limitation that the device is a SONOS device. For the reasons described in this section, the device of Luoh et al. is not a SONOS device.

Claims 20-21, 24, 26, 27, 30-31, and 34 similarly all include the limitation that the device is a SONOS device or a SONOS transistor, and thus distinguish over the floating gate device of Luoh et al.

Thus Luoh et al. fail to teach each and every limitation of claims 9, 12-15, 20-21, 24, 26, 27, 30-31, and 34, and Applicants respectfully request that the 102(e) rejections of these claims be withdrawn.

B. Claims 3, 5-7, 22-23, 25, 28-29, 32-33, and 36-42; 103(a) Rejection: Discussion

Claims 3, 5-7, 22-23, 25, 28-29, 32-33, and 36-42 are rejected under 35 USC 103(a) as being unpatentable over Han et al., US Patent No. 5,700,699 in view of Yu et al., US Patent No. 6,184,155, and Luoh et al.

Claim 3 recites a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

Han et al. shows a thin film transistor having an oxide layer between the gate conductor and the channel, wherein the oxide layer is *not* formed by an ISSG process. The Examiner states:

> But Yu reference discloses the oxide layer 4b fig. 3 column 3 line 32 by ISSG. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to combine the oxide layer 4b by ISSG of Yu to replace the method of making layer 12 of Han, because it would have created a thin gate oxide layer with reduction in leakage current, during standby, or operating modes as taught by Yu, see abstract.

The Examiner rejects claims 23, 25, and 36-42 using the same rationale.

The device of Han is a TFT device used as the driving circuit in an LCD device (col. 1, lines 19-20.) When standard thermal oxidation is used to form the gate oxide for this TFT device, an expensive substrate must be used which can tolerate the high processing temperatures required by this oxidation (col. 1, line 65 – col. 2, line 1.) One object of the invention is to use a low-temperature method to form the gate oxide (see abstract), allowing a cheaper substrate material to be used (col. 4, lines 6-10.)

The single oxide layer used in most embodiments of Han et al., and the bottom oxide of the ONO stack in the embodiment of Fig. 4 of Han et al., is formed using ECR (Electron Cyclotron Resonance) oxygen plasma (col. 3, lines 10-11, *inter alia.*) The formation of oxide layers by ECR oxygen plasma allows the process to be performed at a relatively low temperature. The temperature can be kept below 600 degrees C (col. 3, lines 63-64.)

The oxide layer of Yu et al., however, is formed using a two-step ISSG process, including a thermal oxidation step performed between 600 and 800 degrees C and an anneal step performed between 800 and 1000 degrees C (col. 3, lines 23-30.) The high temperatures required to form the ISSG oxide layer of Yu et al. would exceed the thermal limitations of the device of Han et al. Thus Applicant respectfully submits that it would not be obvious to use the ISSG-produced oxide of Yu et al. in the device of Han et al.

The rejections of claims 5-7 similarly rely on a combination of Han and Yu which is not obvious for the reasons just described.

Applicants also wish to note that, although the embodiment of Fig. 4 of the device of Han et al. includes an ONO stack between a silicon channel and a silicon control gate, this device is technically not a SONOS device. As described in Exhibits A-E described in section A.1, a SONOS device is a memory cell which stores charge in a nitride layer between two oxide layers. The device of Han et al. is nowhere described as a SONOS device, and it is not a memory cell. There is no mention of its use as a memory cell, and the ONO stack is just one option which can replace the more usual option, a single oxide layer, as in the embodiment of Fig. 5 of Han. The single oxide layer cannot store charge and cannot operate as a memory cell. The tunneling oxide, nitride, and blocking oxide of a SONOS device are optimized for this purpose: the tunneling oxide (the oxide adjacent to the channel) is a thin, high-quality oxide intended to allow charge carriers to tunnel through it when charge is applied to the gate, but to prevent escape of charge carriers from the nitride layer when no charge is applied; the nitride layer is relatively thick to maximize charge trapping; and the blocking oxide (adjacent to the control gate) is relatively thick, to prevent *any* migration of charge carriers. Given that a) the device of Han et al. is not identified as a SONOS device and does not function as a memory cell, b) no such optimization of the layers of the ONO stack is identified, and c) the ONO stack is clearly considered to be interchangeable with a single oxide layer, it is apparent that the device is not intended to act as a memory cell and is not in fact a SONOS device.

Claim 22 recites a method for making a gate dielectric structure for a thin film transistor or a SONOS device, comprising providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region, an oxide layer of a gate dielectric

structure by an in-situ steam generation process performed at a temperature ranging from about 600 to about 1050 degrees Celsius, a pressure ranging from about 100 millitorr to about 760 torr, and for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, wherein the device is a thin film transistor or a SONOS device.

The Examiner says "the combination of Han, Yu and Luoh discloses all the limitations of claim 22." Applicants have explained why the combination of Han et al. and Yu et al. is not obvious. It has been explained that Luoh et al. is neither a TFT nor a SONOS device; without further explanation, Applicants cannot determine what elements of Luoh et al. are intended to contribute to the combination.

Regarding claim 28, which depends from claim 3, the Examiner maintains that "Han discloses a method wherein the transistor is a SONOS transistor ..." As described, the device of Han does not include an oxide layer created by ISSG, and the combination of the ISSG process of Yu et al. is not obvious. Further, as describe earlier, the device of Han et al. is not a SONOS device.

Regarding claims 29, 32 and 33, all three of the claims include the limitation that the thin film transistor comprises a floating gate. The Examiner maintains that "Han discloses a method wherein the transistor is a SONOS transistor, wherein the transistor comprises a floating gate 7." As described throughout Han et al., layer 7 is a control gate, not a floating gate. A control gate is used to apply charge to the transistor to turn the transistor on, while a floating gate is an electrically isolated conductive layer that stores charge. No floating gate appears in any of the embodiments of Han et al., nor is the term used at any point in the reference.

In addition, Applicants must reiterate that a SONOS transistor does not and cannot comprise a floating gate. A floating gate device stores charge in a floating gate, which is formed

of a conductive material, typically doped polysilicon. A SONOS device stores charge in a dielectric layer, typically a nitride layer.

Regarding claims 36 and 37, the Examiner asserts that it would have been obvious to use the oxide layer produced by ISSG of Yu et al. to replace the oxide layer 12 of Han et al. Applicants have explained in the response to the rejection of claim 3 why such a substitution is not obvious.

CONCLUSION

In view of these amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. **If any objections or rejections remain, Applicants respectfully request an interview to discuss the references.** If the Examiner has any questions, he is asked to contact the undersigned agent at (408) 869-2921.

April 23, 2004
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Silicon-Nitride as a Tunnel Dielectric for Improved SONOS-Type Flash Memory

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***Abstract*—High-quality silicon-nitride (Si_3N_4) formed by rapid thermal nitridation is investigated as the tunnel dielectric in a SONOS-type memory device for the first time. Compared to a conventional thermal SiO_2 tunnel dielectric, thermal Si_3N_4 provides 100× better retention after 1e5 P/E cycles and better endurance characteristics with low programming voltages. Hence, the SONNS structure is promising for nonvolatile memory applications.**

***Index Terms*—Charge trap, flash memory, silicon nitride, SONNS, SONOS, tunneling.**

I. Introduction

THE SONOS (polysilicon–oxide–nitride–oxide–silicon) memory device has received a lot of attention due to its advantages over the traditional floating-gate flash EEPROM device. These include reduced process complexity, lower voltage operation, improved cycling endurance, and elimination of drain-induced turn-on [1]–[4]. In a conventional SONOS memory device with SiO_2 tunnel dielectric, the electrons and holes must tunnel through 3.15 eV and 4.5 eV energy barriers, respectively, to be injected into the SiN_x trapping layer. Reducing the SiO_2 tunnel layer thickness improves the programming speed, but at the expense of reducing the retention time. Stress-induced leakage current degrades the retention time further. A low-barrier tunnel dielectric is necessary to improve the programming speed with the possibility of increasing the retention time if the tunnel dielectric can offer lower gate leakage current and reduced stress-induced leakage current compared to the SiO_2 tunnel dielectric. High quality Si_3N_4 is a candidate for such a dielectric.

JVD silicon-nitride (Si_3N_4) has recently been demonstrated to be a promising tunnel dielectric for improving the programming speed and lowering the programming voltage of a floating-gate flash memory device [5]. It has been predicted that silicon nitride could be used as tunnel dielectric in trap-based memories [6], [7]. To date no experimental results have been reported. In this paper, a SONOS-type flash memory device was fabricated using thermal nitride grown by rapid thermal nitridation as the tunnel dielectric. The SONNS (polysilicon–oxide–nitride–nitride–silicon) memory device is compared against the conventional SONOS memory device in terms of programming speed, endurance and retention time, and found to have significantly superior performance.

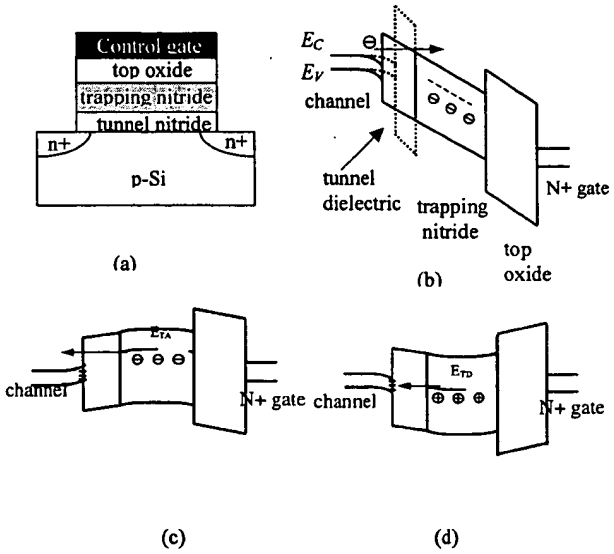

Fig. 1. (a) Schematic cross section of the SONNS memory device. The tunnel dielectric is thermal oxide in the control (SONOS) memory device. (b) SONNS energy band diagram during programming. The dashed lines correspond to the case of a SiO_2 tunnel dielectric, for comparison. The injection barrier is lower for a nitride tunnel layer, so that fast programming speed can be achieved even if the nitride tunnel dielectric is slightly thicker. The situation is similar during erasing. (c) Energy band diagram dubring retention of electrons. (d) Energy band diagram during retention of holes. E_{TA} (~1 eV) and E_{TD} (at middle gap) are the electron and hole trap energy levels in the interlayer nitride, respectively.

II. Device Principle and Fabrication

Fig. 1(a) shows the structure of the SONNS memory device. Programming and erasing are achieved by pulsing the gate voltage to induce electron and hole tunneling, respectively, from the Si substrate into traps located within the interlayer nitride. (Source, body, and drain regions are grounded during programming/erasing and retention.) The energy band diagrams during programming and retention are shown in Fig. 1. During programming/erasing, the electric field across the tunnel dielectric is very large (10 MV/cm); the tunneling current depends strongly on the tunneling barrier height. In retention mode, the electric field depends strongly on the tunnel dielectric thickness. Since the nitride barriers are only 2.1 eV for electrons and 1.9 eV for holes, fast programming/erasing speed can be achieved with direct tunneling in the SONNS device, even if the tunnel nitride is physically thicker than the tunnel oxide in the control SONOS

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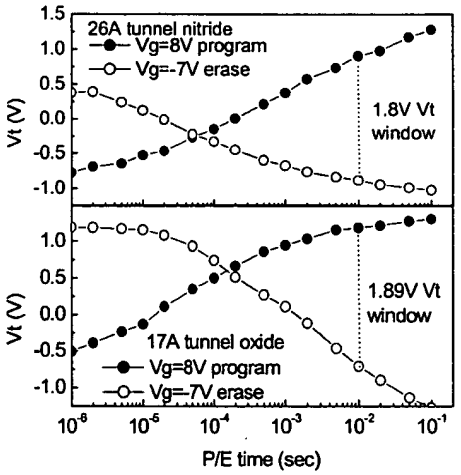

Fig. 2. Program/erase characteristics of fabricated SONNS and SONOS memory devices. The SONNS memory device can achieve comparable V_t window with 10 ms P/E times, although the tunnel nitride is thicker than the tunnel oxide.

device. Since the electric field in the tunnel dielectric is relatively small (~1 MV/cm) during retention [8], the thicker tunnel nitride can effectively block electrons and holes from leaking back to the channel, resulting in longer retention time.

N-channel SONNS and SONOS devices were fabricated using a conventional process with LOCOS isolation. The 2.6 nm tunnel nitride in the SONNS memory devices was formed by rapid thermal nitridation (RTN) at 1100 °C in NH_3 ambient. The 1.7 nm tunnel oxide in the control SONOS devices was grown at 800 °C in dilute O_2 (10%) ambient. The 5 nm Si_xN_y (x:y = 4:5 determined by Auger Electron Spectroscopy) charge-trapping interlayer was formed by low-pressure chemical vapor deposition (LPCVD) at 750 °C. The etch rates for the trapping nitride and the tunnel nitride in 5:1 BHF were found to be 1.5 nm/min and 0.35 nm/min, respectively. The slower etch rate of the tunnel nitride confirms that it is of higher quality. The top oxide was 4 nm high-temperature oxide (HTO) deposited at 800 °C and densified in a steam ambient at 800 °C for 20 minutes. The data reported in this paper are for devices with $W/L = 2\ \mu m/0.4\ \mu m$.

III. Results and Discussion

The program/erase (P/E) characteristics for SONNS and control SONOS memory devices are shown in Fig. 2. The channel doping in the SONNS device is lower than in the SONOS device because of dopant diffusion during the high-temperature RTN process; thus, the intrinsic V_t values are slightly different. However, the V_t windows are comparable: for 10 ms P/E pulse time, the V_t windows are 1.80 V and 1.89 V for the SONNS and SONOS devices, respectively.

Endurance characteristics are shown in Fig. 3. The SONNS memory device maintains a wide V_t window even after 10^6 P/E cycles. In contrast, the SONOS device shows more degradation than the SONNS device after P/E cycles. The V_t shift upward is due to interface-trap generation. Retention characteristics at 85 °C are shown in Fig. 4. For a 0.5 V V_t window, a fresh SONNS device achieves 10^7 seconds retention time, as compared to 3×10^6 s for the SONOS control device. The thicker tunnel dielectric in the SONNS device provides for better elec-

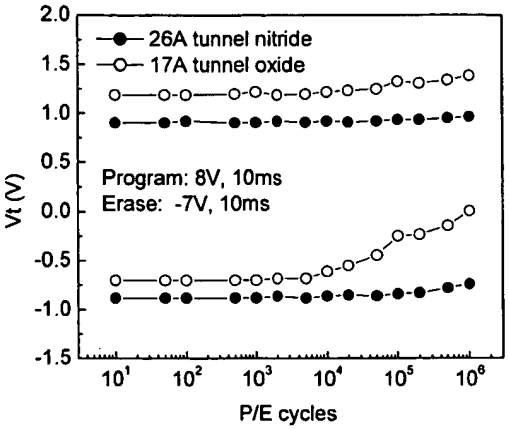

Fig. 3. Endurance characteristics of fabricated SONNS and SONOS memory devices. The SONNS memory device shows little degradation even after 10^6 P/E cycles, while the SONOS memory device shows more degradation after P/E cycles.

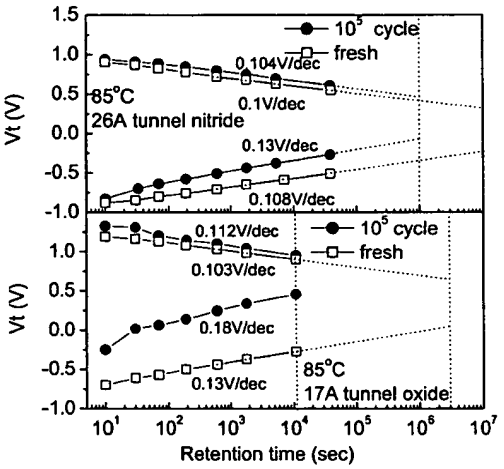

Fig. 4. Retention characteristics. (a) SONNS memory device: for a 0.5 V V_t window, the retention time is better than 10^7 seconds in a fresh device, and 10^6 s after 10^5 P/E cycles. (b) SONOS memory device: for a 0.5 V V_t window, the retention time is 3×10^6 s in a fresh device and only 10^4 s after 10^5 P/E cycles.

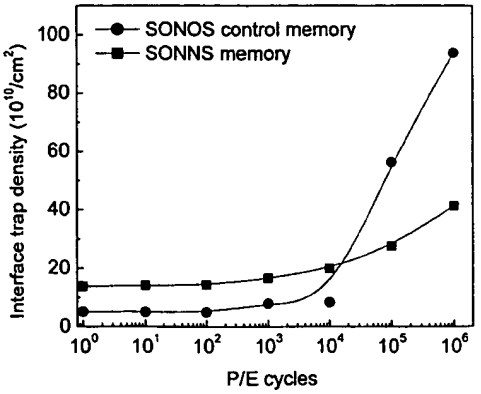

Fig. 5. Interface trap density determined by the charge-pumping technique. The tunnel nitride is more robust against interface-trap generation: the trap density in the SONOS device exceeds that in the SONNS device after 10^5 P/E cycles.

tron and hole retention. It should also be noted that, for a given electric field at the Si surface, the electric field in the tunnel nitride layer is smaller than in the tunnel oxide layer because of the higher permittivity of nitride. After 10^5 P/E cycles, the SONNS device can still maintain a $\geq$0.5 V V_t window after 10^6 s, whereas the retention time of the SONOS memory device degrades to 10^4 seconds. In the SONNS device, the hole loss rate after 10^5 P/E cycles increases only slightly compared to that of the fresh device, while it increases significantly (from 0.13 V/dec. to 0.18 V/dec.) in the SONOS device. Erased-state retention is related to interface trap density, since trapped holes can tunnel out of the interlayer nitride to available interface trap states, as shown in Fig. 1(d). The evolution of interface trap density (determined using the charge-pumping technique) with the number of P/E cycles is shown in Fig. 5. Although the initial interface trap density is higher for the tunnel nitride, it is more robust against interface trap generation, so that better hole retention is ultimately seen in the SONNS device.

IV. Conclusion

High-quality nitride is applied as the tunnel dielectric in a SONOS-type memory device for the first time. For comparable program/erase speed, the endurance of a SONNS device is better than for a SONOS and the retention time of a SONNS device is 100× superior than that for a SONOS device after 1e5 cycles. This is due to the quality of the thermal nitride, its robustness against interface trap generation and the lower electric field in the nitride during programming/erasing. High-quality nitride is therefore a promising tunnel dielectric for future flash memory technology, although thicker tunnel nitride is required for ten years retention time.

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Impact of Nitride Process Conditions on SONOS Flash Devices

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ABSTRACT

SONOS (Silicon-Oxide-Nitride-Oxide-silicon) Flash memory has the potential to replace most memory products in the future. However, there are technical problems remain to be solved in the course of developing high-capacity memories. In this work, various process conditions and their influences on device characteristics have been carefully examined and evaluated for possible solution of Gbit solid-state memories. Experimental results indicate that silicon-rich nitride layer has lead to high charge-trapping efficiency and baking process can improve leakage significantly. The research conclusion could provide useful experience and information in process and structure design for Gbit SONOS flash memory applications.

Keywords : SONOS, flash memory, charge-trapping efficiency

氮化矽製程條件對 SONOS 快閃式記憶體元件之影響

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摘 要

SONOS 結構之快閃式記憶體未來有取代大部分記憶產品之潛力；然而在高記憶容量技術的發展過程當中，仍有許多瓶頸尚待克服。本論文中，研究各種不同的製程條件並審慎評估其對元件之影響，期能提供製作十億位元固態記憶體之參考。實驗結果顯示在氮化矽層中提昇矽與氮的相對含量將有效提昇元件的電荷捕捉效率；此外，實驗數據亦指出烘烤效應能明顯的改善漏電流的特性。本研究結論對十億位元 SONOS 快閃式記憶體之製程條件與結構設計當可提供有用之經驗與資訊。

關鍵詞：SONOS，快閃式記憶體，電荷捕捉效率

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I. INTRODUCTION

The rapidly growing market share of memory devices has brought about competitive development of memory technologies. Among various designs, Flash memory has become extremely attractive due to its significant advantages such as non-volatility, repetitive electrical program/erase capability, shock resistance, low power consumption, high endurance, and long retention [1-6]. However, the high-voltage operation requirement and the scaling limit in pushing memory density towards Gbit level have prompted the search of new Flash memory design. In one promising structure, SONOS, the silicon nitride thin film as a replacement of conventional floating gate has been adopted to reduce operation voltage and increase storage density [7-11]. The insulating property of nitride layer has made it possible to scale down the dielectrics further and allows dual-bits-per-cell operation mode [12]. Additionally, SONOS Flash exhibits superior resistance to radiation in contrast to conventional Flash memories [13,14]. In spite of its advantages, there are some reliability issues such as program window decay that need to be resolved before its full-scale replacement of other memory products can be realized. In this work, the influence of nitride process condition such as silicon content ratio control and post-fabrication treatment such as UV exposure and baking on SONOS device performance has been studied.

II. IMPLEMENTATION

The SONOS Flash test devices are fabricated by standard CMOS process on p-type substrate except the ONO structure formation and the key process steps of the dielectrics are described as follow. A 2.8-nm thick tunnel oxide was formed by Low-Pressure Chemical Vapor Deposition (LPCVD) with gas flow ratio of SiH_2Cl_2:N_2O = 10:100 (sccm) at 725℃. Next, a 4.5-nm thick silicon nitride was deposited in a LPCVD reactor under various process conditions. The 4.0-nm thick LPCVD blocking oxide was deposited on top of nitride with same gas flow ratio and temperature as tunnel oxide. The polysilicon deposition and the rest of the process simply followed standard CMOS procedure. For the ease of comparison, both capacitors and transistors have been fabricated and the cross section of the finished SONOS test structure is shown in Fig. 1.

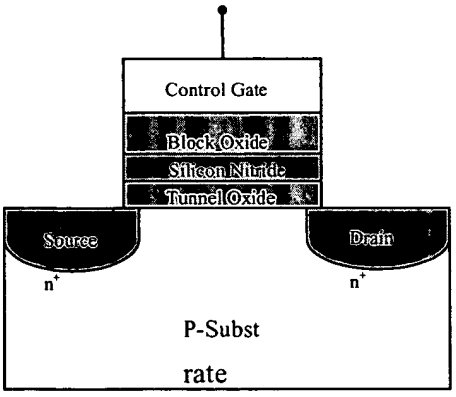


Fig.1. Cross-section view of the SONOS devices.

After the test devices were fabricated, some wafers were illuminated with UV light as standard EEPROM devices would usually be treated and some were also baked for later

comparison. The key processing conditions of the nitride layer and the treatment of finished devices are listed in table I.

Table I. Key process and treatment conditions.

Wafer #	Temp (℃)	SiH_2Cl_2/NH_3 Flow Ratio	UV Exposure	Baked	Si content	wafer name
1	790	1 : 10			3	1
1	790	1 : 10		V	3	1B
2	730	1 : 10	V		2	2UV
2	730	1 : 10	V	V	2	2UVB
3	730	1 : 10			2	3
3	730	1 : 10		V	2	3B
4	730	3 : 10			1	4
4	730	3 : 10		V	1	4B

In order to study the influence of various process conditions and treatments on device performance, both DC I-V and high-frequency C-V characteristics have been extracted by a Keithley Semiconductor parameter analyzing system. The electrical characteristics of test devices are mainly utilized to evaluate the leakage and charge-trapping efficiency of SONOS devices.

III. RESULTS AND DISCUSSION

Figure 2 shows the I-V characteristics of SONOS transistors with channel length varies from 0.6m to 10m. It has been verified that Fowler-Nordheim (FN) tunneling mechanism becomes dominant under bias above +10 V and below –7V as demonstrated in the inset of Fig. 2. The smaller slope of the I-V curve within FN-tunnel regime on the left-hand side indicates a lower hole-injection efficiency and hence slower program/erase under negative bias. In addition, channel length has negligible effect on leakage or tunneling characteristics.

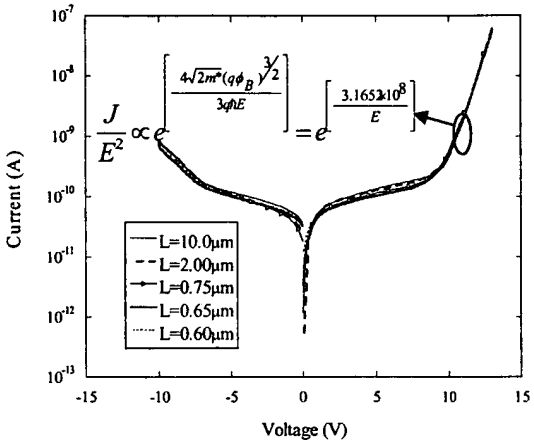


Fig.2. I-V characteristics of transistors with various channel length on test wafer #2.

On the other hand, UV illumination that is used to drive out residual charges in the trapping layer has raised the leakage level by one order of magnitude as shown in Figure 3. The leakage increment may be attributed to the increased defects induced by UV exposure in the tunnel oxide. For further investigation of the influence of UV-illumination on device reliability, the time-dependent leakage behavior of SONOS capacitors (240m × 240m) under constant voltage stress (CVS) has been monitored.

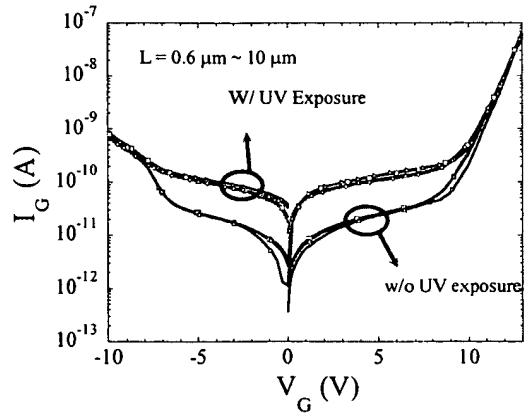


Fig.3. Comparison of I-V characteristics of transistors on test wafer #2 and #3 with and without UV exposure.

Figure 4 shows that the leakage increases significantly after UV exposure. Under positive bias, the initial electron-trapping state even progressively changes into hole-trapping state. This result implies that UV illumination has lead to grown defect (stress-induced hole trapping sites) number in dielectrics and hence oxide degradation that raises leakage level. As a result, data retention time of SONOS devices would be shortened and that is detrimental to long-term data storage. Fortunately, UV exposure-induced leakage can be improved by post-baking treatment.

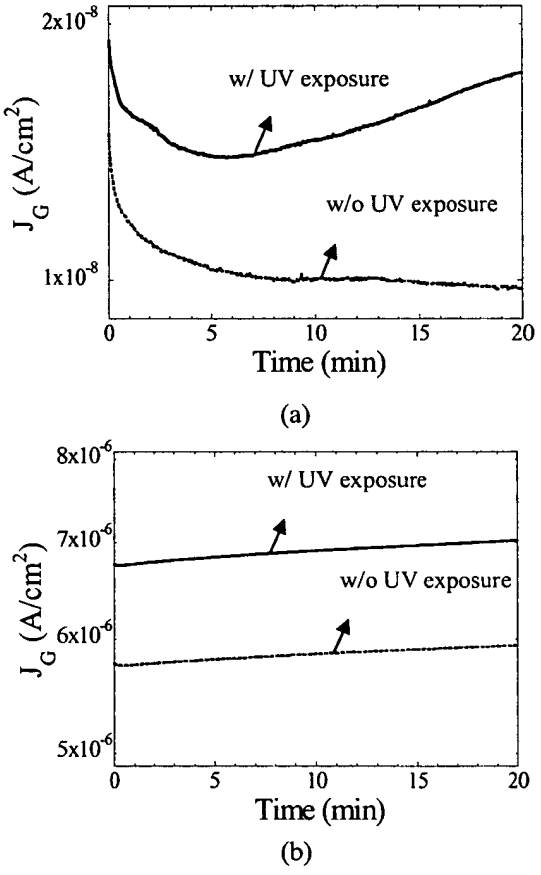


Fig.4. Comparison of J-t characteristics of capacitors on test wafer #2 & #3 under (a) +13 V and (b) –7 V constant voltage stress.

Figure 5 shows that a 250 ℃, 10 hr baking treatment of test devices illuminated by UV light has resulted in a significant leakage reduction. The baking treatment also improves leakage characteristics of the test devices without UV exposure. It is believed that the process-induced defects in the as-deposited dielectrics can be cut down through baking procedure.

For semiconductor memory devices, leakage and charge-trapping efficiency are two major parameters considered in device performance evaluation. Charge-trapping efficiency determines if the memory devices can keep enough charges in the storage nodes after program/erase operation and is reflected in retention characteristics. It is especially critical when the leakage behavior of storage devices is inevitable. For SONOS devices, the nitride layer is responsible for trapping charges and its efficiency in this study is assessed by I-V characterization of transistors and C-V measurement of capacitors.

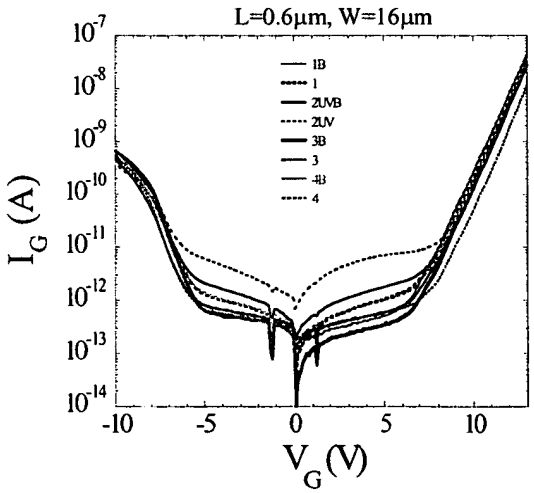


Fig.5. Comparison of I-V characteristics of transistors on all test wafers before with and without baking treatment.

I-V characterization records threshold voltage shift (V_T) of transistors while C-V measurement marks down flatband voltage variation (V_{FB}) of capacitors after program/erase operation. Figures 6 and 7 show the V_T of transistors and V_{FB} of capacitors on UV-illuminated test wafer #2 respectively after program/erase operation. Since V_T and V_{FB} are both proportional to charge-trapping efficiency, they can be used to evaluate the influence of various nitride deposition conditions on SONOS device performance. It is found that under same program/erase operation voltage, V_T and V_{FB} vary if the initial biasing point of reading operation differs. For example, V_T shift towards the left is less if the initial bias is –4 V than that with initial bias of –10 V after –10 V program operation. The variation of V_T and V_{FB} with different initial bias of reading operation can be attributed to the leakage characteristics of SONOS device where a certain amount of charges run off from nitride layer after program/erase.

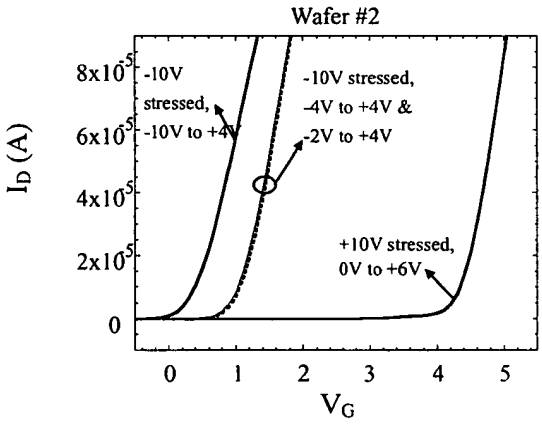


Fig.6. V_T shift of transistors on wafer #2 after program/erase operation by I-V measurement.

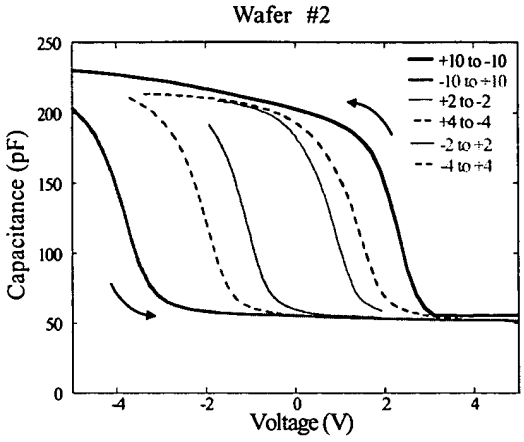
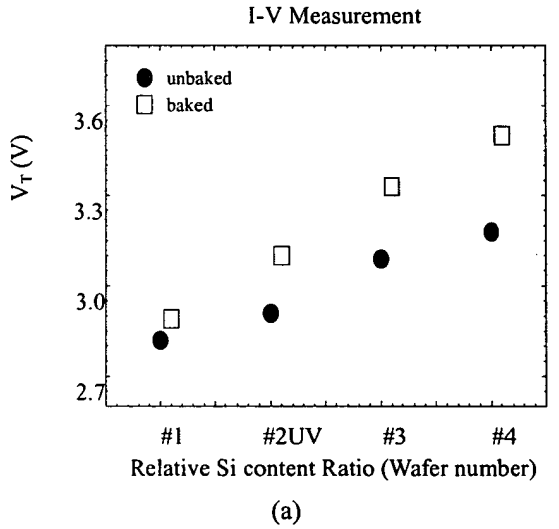


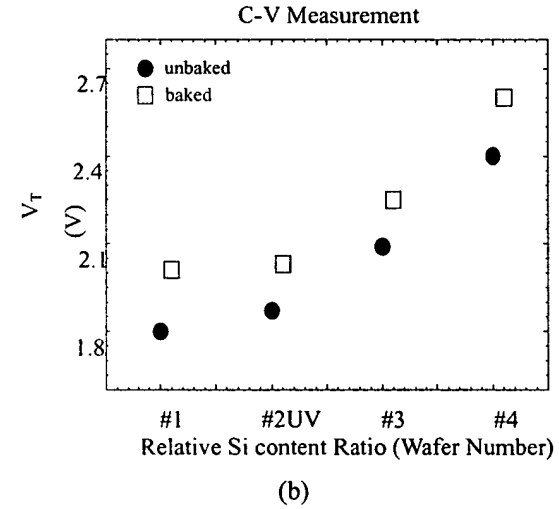
Fig.7. V_{FB} shift of transistors on wafer #2 after program/erase operation by C-V measurement.

Based on V_T and V_{FB} data of all test devices, important trend of processing conditions can be concluded. The relative silicon content in the nitride layer increases with higher SiH_2Cl_2/NH_3 flow ratio or lower temperature [15,16]. Therefore, it can be deduced that the nitride on test wafer #1 contains least silicon content while the nitride on test wafer #4 contains most relative silicon content ratio in table I. The nitride on test wafer #2 and #3 contains same silicon content which is between those on wafer #1 and #4. Experimental data in Fig. 8 show that V_T and V_{FB} increase from wafer #1 to #4 which implies that the charge-trapping efficiency is proportional to relative silicon content ratio in nitride layer. UV exposure has reduced the trapping efficiency while baking treatment has improved the trapping efficiency for all cases. Although silicon content plays an important role in charge-trapping efficiency, it does not have same constructive effect on leakage characteristics. In fact, the leakage level of the

devices on wafer #4 exceeds those on wafer #3. Further study is required to reveal the influence of silicon content on leakage level. The optimum process conditions can be determined based on the analysis procedure described above and they would be very useful in improving SONOS device characteristics.



(a)



(b)

Fig.8. V_T shift of transistors in correspondence with relative silicon content by (a) I-V measurement and (b) C-V measurement.

IV. CONCLUSION

In summary, we have studied various process conditions of nitride layer in SONOS memory devices. It is seen that the relative silicon content has significant influence on device charge-trapping efficiency. A Si-rich nitride film tends to exhibit higher charge-trapping efficiency. However, it might lead to elevated leakage if exposed to UV illumination. Fortunately, baking treatment could amend such flaw. From the above results, silicon-rich nitride with baking treatment has proven to be the most promising candidate for SONOS Flash memory application due to its high charge-trapping efficiency and low leakage..

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PROFILE
TECHNOLOGIES A-Z
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BUSINESS INITIATIVES

Embedded non-volatile memories

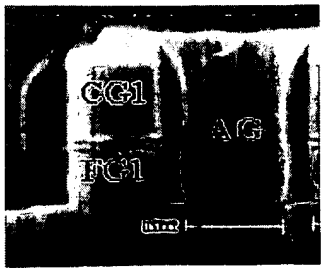
Introduction

Embedded memories are becoming more and more important in today's IC technology. The embed a memory onboard a standard CMOS chip instead of using a multi-chip solution (witl logic and memory chips) is for instance motivated by the higher data transmission speed, tl power consumption, security issues, cost reduction, or just by the smaller module size. The embedded memory group at PRLe is mainly on one of the many varieties of embedded mer ***embedded non-volatile memories***. By definition, a non-volatile memory is able to retain data for a long period of time (at least ten years) without any power supply. Consequently, memory is ideally suited for both program code and for data storage, which explains why or embedded non-volatile memories in a very wide field of products, ranging from smart cards communication IC's. Obviously, it is very important to have the embedded flash option avai shortly as possible after the launch of each new CMOS process. For example, the ***CMOS18F*** (embedded flash option to the 0.18 µm CMOS process, flash cell size = 0.78 µm²) was one 0.18 µm embedded flash processes available on the market. Below, two of the concepts tha in Leuven to ensure this leading role also for the future are discussed.

The compact poly-CMP cell

As for most integrated devices, a smaller memory cell size implies lower fabrication costs, a cell size down-scaling is of uttermost importance. Apart from the cell size, other key parame embedded memories are the required programming voltages (determining the power consu the final product), the read current (determining the speed of the memory), and the ease o in a standard CMOS process (i.e., the costs of adding a non-volatile memory function to the Unfortunately, a straightforward adaptation to fit the successful 2-transistor flash concept (i production in the 0.18 µm CMOS generation) in advanced process generations, such as the CMOS node, is not without problems. First of all, the cell size would not shrink by the expec 4, but only by appr. 3x. Furthermore, the lithography of the scaled 2-transistor cell would b troublesome, even with state-of-the-art equipment.

Therefore, besides studying the possibilities of the scaled 2-T cell, we also look for new non-volatile memory cell concepts, one of which is the ***compact poly-CMP cell*** (Philips IP), of which an example is shown in the cross-section electron microscope picture in *figure 1*. Basically, in the compact poly-CMP non-volatile memory cell, two separate transistors, one selection transistor and one storage transistor, are merged into one single 'long channel' device, thereby improving the overall scalability. The data are stored as electrons on the floating gate, and read-out is based on the fact that the stored electrons modulate the threshold voltage V_T of the storage transistor (the difference between a '0' and a '1' corresponds roughly to 1000 - 100 electrons).



The storage density can even be increased further by using the double variant of the compact poly-CMP cell, a prototype of which is depicted in Figure 2. In such a double cell, three transistors, two storage transistors and a selection device, share one common channel. The price to be paid for the higher density is that programming and reading is more complex, since the two stored bits should be 'separated'.

SONOS memories

SONOS, which stands for Semiconductor-Oxide-Nitride-Oxide-Semiconductor, is a memory which was invented as long ago as the 1960's, but the concept was abandoned in the 1980' technological issues. Nowadays, these technological barriers have been overcome to a great catalysed by the improved semiconductor fabrication methods. This has led to a revival of ir SONOS devices, mainly driven by the better scaling perspectives and the ease of integration line CMOS process, compared to standard floating gate memories. Moreover, some perform parameters, such as the write/erase endurance and the required programming voltages, ex of flash memories.

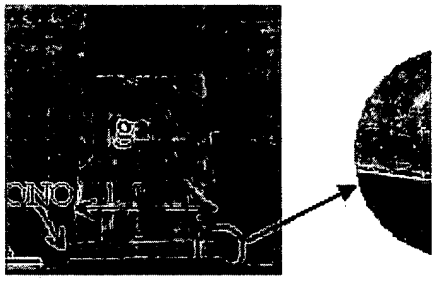
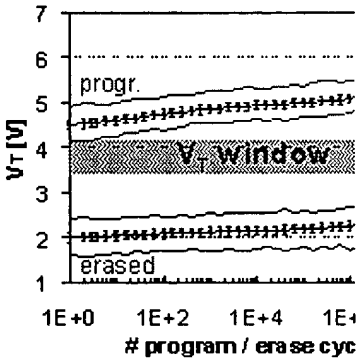


Figure 3 shows a cross sectional view of a SONOS memory cell, made with a transmission electron microscope. Essentially, the cell is a conventional NMOS transistor, but with a gate dielectric consisting of a thermal oxide layer of approximately 2 nm thickness, a silicon nitride layer of about 5 nm and a second oxide layer with a thickness between 5 and 10 nm. At a positive gate bias, electrons can tunnel from the substrate through the ultra-thin oxide layer to the nitride layer, where they are subsequently trapped (silicon nitride has the intrinsic property to trap electrons). Due to this trapped negative charge, the voltage of the transistor increases. Likewise, the threshold voltage can be decreased with a voltage on the gate, expelling the electrons from the nitride layer. So, roughly speaking, the layer takes over the role of the floating gate in a standard flash cell.

The process of programming and erasing can be repeated many times, as is demonstrated in Figure 4, showing the programmed and erased V_T of a medium-sized SONOS array (26 kbit) during as much as 100 million (!) cycles. Although the characteristics slightly change upon program/erase cycling (for instance due to permanent electron trapping in the ONO stack), the endurance is more than two orders of magnitude better than that of standard flash memories.



Design Considerations in Scaled SONOS Nonvolatile Memory Devices

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Abstract — Scaling the programming voltage, while still maintaining 10-year data retention time, has been always a big challenge for Poly-Oxide-Nitride-Oxide-Silicon (SONOS) researchers. We describe our progress in the design and scaling of SONOS nonvolatile memory devices. –9V +10V (1ms) programmable SONOS devices ensuring 10 years retention time after 10^7 Erase/Write cycles at 85°C have been developed successfully. Deuterium anneal, applied in SONOS device fabrication for the first time, improves the endurance characteristics better than traditional hydrogen or forming gas anneal. In this paper, we describe scaling considerations and process optimization along with experiments and characterization results.

TABLE OF CONTENTS

1. INTRODUCTION

Next generation high density electrically erasable programmable read-only memories (EEPROMs) require an endurance in excess of 10^6 erase/write cycles with 10-year data retention at 85°C and low programming voltages 5-10V [1] [2]. Two basic types of EEPROMs exist, namely, the floating gate device and the floating trap device, i.e. SONOS [3-4]. The floating gate device stores charge in the polysilicon as free carriers as a continuous spatial distribution in the conduction band, and the SONOS stores charge in spatially isolated deep level traps (Fig. 1).

The floating-gate memory has been running out of steam with respect to scaling cell-size and program/erase voltages. The relatively thick (7-12 nm) tunnel oxide in the floating-gate type memories provides good 10-year data retention; however, the high voltage requirement [5] has created a reliability issue, as it has exceeded the voltage limits of scaled CMOS devices. Dielectric hot carrier degradation, punch-through avalanche effects and high voltage junction breakdown [6-8] limit the lateral scaling to achieve high density. The concern over the loss of the entire memory charge through a single defect in the tunnel oxide limits vertical scaling and lower programming voltages [2], which increases support circuitry area and reduces the array efficiency.

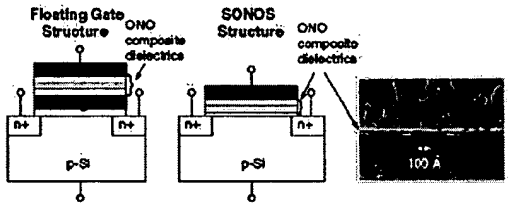

Fig. 1 Floating gate memory and floating trap (SONOS) with device cross-section.

The demand for low-power, low voltage electronics has accelerated the pace for NVSM circuit designers to consider SONOS for low voltage, high density EEPROM's. The motivation for the interest in SONOS lies in low programming voltages, endurance to extended erase/write cycling, resistance to radiation, and compatibility with high density scaled CMOS technology. A 3V, 1Mb, full-featured SONOS EEPROM has been manufactured using 0.8 μm CMOS technology [9]. Fujiwara et al. reported a 0.13 μm SONOS single transistor memory cell [10] with unselected word line bias for program-disturb improvement with subsequent scaling to 0.1 μm and beyond [11].

A radiation-hardened, SONOS based 4K gate field programmable gate array (FPGA) device has been described in 0.8 μm triple-level metal technology [12]. In this array SONOS transistors provide program connectivity and, for the first

time, offer the feature of reconfigurability in a FPGA device. SONOS NVSMs are capable of a small cell size ($6F^2$ where F = feature size) [13]. The ultra-thin tunnel oxide can conduct high current via direct tunneling with less charge trapping and a dramatic increase in charge-to-breakdown, Q_{BD}, with tunnel oxide thickness less than 3.2 nm – the mean free path of electrons in the oxide. Thus, we have the possibility of thin tunnel oxide SONOS devices for dynamic/quasi-nonvolatile memory applications, as discussed by Wann et al. [14] and King et al. [15].

A considerable effort has been devoted to scaling the programming voltages of SONOS devices with improved retention characteristics under extended erase/write cycling at elevated temperatures. Minami and Kamigaki reported a SONOS device with 10-year data retention after 10^7 erase/write cycles with programming voltage –11V +13V (1ms) [16]. Reisinger et al. proposed a p+ gate SONOS structure [17] to improve erase speed and data retention time. Libsch et al. [18], French and White [19], Yang and White [20] have all discussed a 5-8V EEPROM cell for high density NVSM.

Recently, we have explored the scaling of low voltage, long retention SONOS memory devices. SONOS devices fabricated at Lehigh University show a 0.5V detection window at 10-year data retention after 10^7 erase/write cycles at 85°C with programming voltage –9V +10V (1ms). We will describe scaling and process optimization in the Section 2. SONOS device fabrication and characterization results are described in Sections 3 and 4, respectively.

2. SCALING CONSIDERATIONS -- PROCESS OPTIMIZATION--

2.1 ONO Stack Scaling

Three approaches have been described in the literature to obtain good balance between speed, retention and endurance. One approach, taken by Roy and White [21], is to scale the nitride storage layer, but keep the blocking oxide thicker, which increase the memory window (will decrease for scaled nitride layer otherwise) and the amount of charge trapped at nitride/blocking oxide interface is increased too. Another approach, taken by Minami and Kamigaki [15], and Dellin et al. [22], uses a thin blocking oxide just thick enough to block the injection of charge from the gate, and scale the nitride layer at the same time. The other approach, investigated by Williams et al. [23] and Kapoor et al. [24], employed an oxynitride instead of the nitride as the storage medium, because the oxynitride film has a smaller trap density and hence a smaller Coulombic repulsion between the trapped charges. The tunnel oxide can be further scaled with or without a blocking oxide. In addition, Hu and White [25] have presented a buried channel device instead of a surface channel device to reduce back tunneling.

The work presented in this paper is based on the first approach, namely, incorporating the optimization of the tunnel oxide thickness [26]. For 8-10V program/erase voltages, a 10 nm effective gate dielectric thickness is preferred to guarantee an electric field for modified Fowler-Nordheim tunneling [27]. A 2.0 nm tunnel oxide and thicker blocking oxide (5.5 nm) are used for good retention and reliability considerations. The scaling of the nitride layer is based on the constant tunnel oxide electric field theory, which we will detail in Section 4 with a comparison of different design approaches.

2.2 Process Optimization

In our scaling, a trap-rich, silicon nitride (with a $SiCl_2H_2$: NH_3 ratio of 10:1) is necessary, as silicon nitride films deposited with high $SiCl_2H_2$: NH_3 gas flow ratios show high trap densities, which facilitate fast programming speed [28]. Yang et al. [29] conducted AFM studies on silicon nitride films, which were deposited at different temperatures. Their studies revealed 680°C as the optimum temperature for LPCVD nitride deposition for a minimum surface roughness with improved memory retention. Minami et al. demonstrated LPCVD formed blocking oxides improved data retention dramatically [15]. In addition, tunnel oxides grown at high temperature, exhibit improved performance and reliability [30]. Superior retention and endurance are obtained with the use of a triple-wall oxidation furnace rather than the conventional single-wall furnace [25].

We have performed high temperature (700°C 4 hours) deuterium anneals instead of hydrogen forming gas anneals after the contact windows are opened. Anneal temperatures comparable to or lower than the nitride deposition temperature provide less migration of the stored charge in the nitride [15]. Also, the interface states generation is reduced under extended program/erase cycling and retention reliability is improved as described in Section 4.

3. SONOS DEVICE FABRICATION

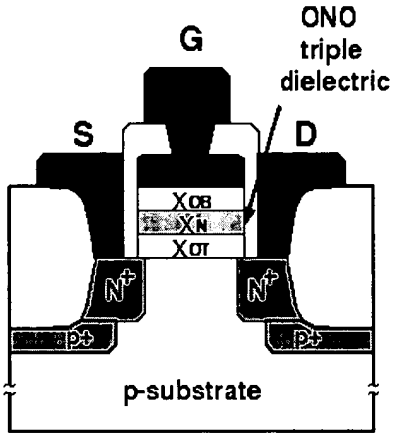

Fig. 2 Device structure of SONOS nonvolatile memory transistor with tunnel oxide 2.0 nm, nitride layer 4.5 nm, and blocking oxide 5.5 nm.

We have fabricated SONOS devices with N-well CMOS technology and LOCOS isolation. The processing sequence is identical to conventional CMOS technology except for the formation of the ONO dielectric stack. The key process steps are as follows: A 2.0 nm thick tunnel oxide is grown at 800°C for 40 min. with argon-diluted oxygen (1% O_2 in Ar) in a custom-designed triple wall oxidation furnace followed by 30 min. argon anneal to relieve the stress caused by high temperature oxidation. Next, a 4.5 nm silicon nitride is deposited in a LPCVD reactor for 15 min. at 680°C with gas flow ratio of $SiCl_2H_2$: NH_3 = 100:10 (sccm). A 5.5 nm LPCVD blocking oxide is deposited with $SiCl_2H_2$: N_2O = 10:100 (sccm) at 725°C followed by a steam densification at 900°C for 30 min. After the ONO triple dielectric film is formed, a layer of polysilicon is deposited and doped in a $POCl_3$ process. Next, the gate is patterned and the contact windows are opened. A 4 hour 10% D_2/N_2 anneal at 700°C is performed to lower the interface state density. This is followed by an aluminum deposition for contact metallization with a post-metal-anneal (PMA) at 400°C for 30 min. in 10% D_2/N_2. For comparison purposes, another group of wafers annealed with 10% H_2/N_2 are fabricated at the same time. Fig. 2 shows the device structure.

4. MEASUREMENT RESULTS AND DISCUSSION

In this section, we present erase/write, retention and endurance electrical characteristics of scaled SONOS devices. The threshold voltage shifts are measured 1 μs after an erase (write) pulse that follows a 10 s low voltage reset pulse of reverse polarity. All measurements are made at 85°C unless specified. We compare the effects of high temperature deuterium and hydrogen anneals.

Fig. 3 shows the erase/write characteristics. The SONOS device can be operated with a 1 ms –9V/+10V pulse. In the +10V write or program operation, the initial electric field across the tunnel oxide is 11.8 MV/cm with 9.8 MV/cm for the –9V erase operation. In previous MONOS/ SONOS scaling scenarios the electric field across the tunnel oxide or nitride has been maintained nearly constant while the triple dielectric dimensions are scaled [31-32]. Using the constant tunnel oxide electric field theory as the criteria, we compared devices scaled along different approaches in Fig. 4. For the device with 1.8 nm tunnel oxide reported by Minami et al. [16], the initial electric field at 13V is approximately 10MV/cm, assuming zero stored nitride charge.

If we scale the nitride from 13 nm to 4.5 nm and thicken the tunnel and blocking oxides to maintain the same initial electric field, then we have a 10 nm effective gate dielectric thickness with a programming voltage decreased to 9V. However, a smaller memory window and earlier saturation are observed with our scaled nitride device. A thicker tunnel oxide and blocking oxide compensates for the barrier lowering effect due to Coulombic repulsion in the scaled nitride layer (associated with degraded retention) and offers highly-reliable retention characteristics. French et al. [27] noticed scaling the blocking oxide does not improve the erase/write speed of the device. Fig. 5 illustrates the retention and endurance characteristics of our device. 10-year data retention with 0.5V memory window after 10^7 erase/write cycles at 85°C is ensured.

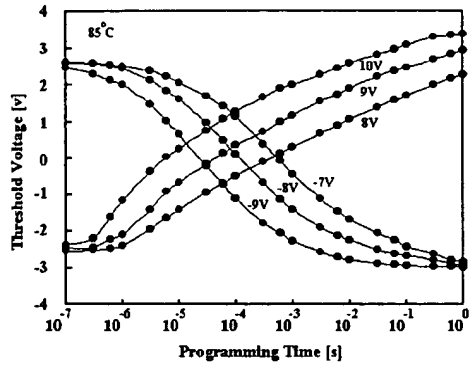

Fig. 3 Erase/write characteristics for scaled SONOS device with tunnel oxide 2.0nm, nitride 4.5nm, blocking oxide 5.5nm.

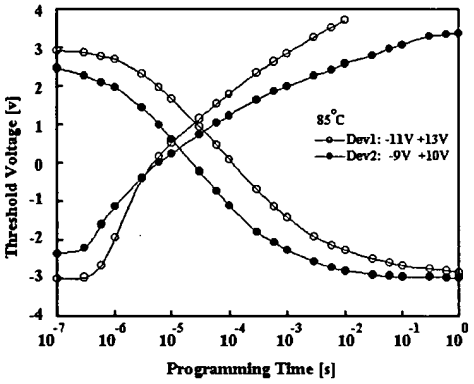

Fig. 4 Comparison of SONOS/MONOS devices with different design approaches. Dev1: tunnel oxide 1.8nm, nitride 13nm, blocking oxide 3nm. Dev2: tunnel oxide 2.0nm, nitride 4.5nm, blocking oxide 5.5nm.

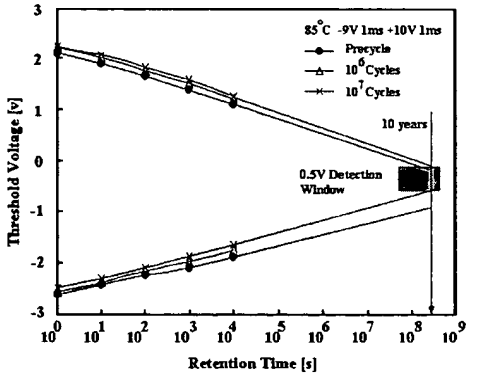

Fig. 5 Retention characteristics after erase/write cycles for SONOS device with tunnel oxide 2.0nm, nitride 4.5nm, blocking oxide 5.5nm.

The deterioration of Si-SiO_2 interface is of major concern in NVSM devices because of the high electric fields across the insulators and the continual passage of charge across the tunnel oxide region. This deterioration manifests itself as a buildup of "interface traps", which are defect centers located at the Si-SiO_2 interface. Their build-up, along with traps exist between SiO_2-Si_3N_4 layer, is detrimental to both SONOS and floating-gate NVSM operation because they (1) provide an additional shift in the device threshold voltage and (2) degrade long-term retention by increasing the so-called back-tunneling current [33]. Maes et al. have employed high temperature hydrogen anneals to reduce interface trap density and improve data retention time [34].

The channel hot carrier lifetime of MOSFETs, annealed in a deuterium ambient instead of the traditional hydrogen or forming gas ambient, have increased by an order of magnitude [35]. In an extension of these studies, we have examined high temperature deuterium anneals in the fabrication of SONOS devices. Fig. 6 compares the interface trap densities (D_{it}) of SONOS devices annealed in deuterium and hydrogen environments. The initial D_{it} is nearly the same for both devices. However, under extensive erase/write cycling, more interface traps are created for hydrogen annealed devices than with deuterium annealed devices.

The retention characteristics of hydrogen annealed SONOS devices are shown in Fig. 7. In contrast with Fig. 5, deuterium annealed SONOS devices have nearly an order of magnitude longer retention time after 10^7 erase/write cycles at 85°C than hydrogen annealed devices for the same detection window. Studies have been conducted to investigate this isotopic interfacial hardening effect [36]. These studies suggest the improved robustness of interface states to dissociation is associated with the difference in vibration mode frequencies of the Si-H and Si-D configurations. The vibration frequency of the bending mode for Si-D bonds is around 460 cm^{-1}, which is very close to the frequency of one of the bulk silicon phonon modes (463 cm^{-1}). Coupling of these modes can provide an energy relaxation channel and make the dissociation of Si-D bonds more difficult than the dissociation of Si-H bonds.

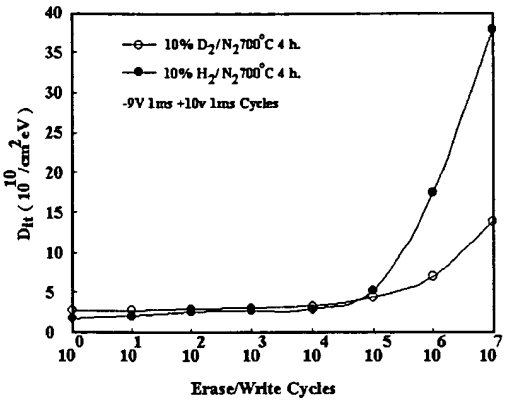

Fig. 6 Dit variation of high temperature deuterium annealed and hydrogen annealed devices.

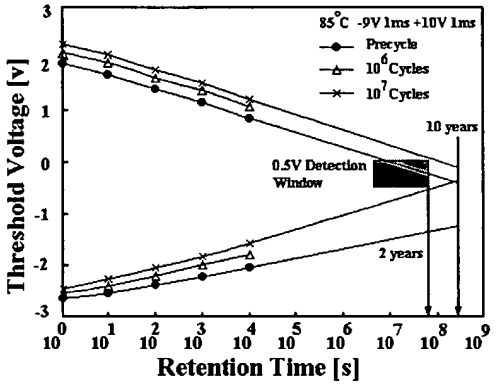

Fig. 7 Retention characteristics of a hydrogen-annealed SONOS device. Compared with deuterium-annealed SONOS in Fig. 5, retention time is nearly one order of magnitude shorter for the same detection window.

5. CONCLUSIONS

SONOS nonvolatile memory devices exhibit a 0.5V detection window with 10-year data retention after 10^7 erase/write cycles at 85°C, with 1 ms +10V/–9V program/erase voltages. Deuterium annealing offers improved endurance characteristics over traditional hydrogen forming gas anneals. These SONOS devices are promising candidates for low voltage, radiation-hardened, high-density EEPROM's applications.

6. ACKNOWLEDGMENTS

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8. BIOGRAPHIES

Jiankang Bu was born in Hebei Province, China on February 4, 1972. He received his B.S. degree (1994) and M.S. degree (1997) in Electrical Engineering from Nankai University, China. He joined the Electrical Engineering Dept. at Lehigh University in the Fall 1997 as a research assistant. He is currently working on his Ph.D degree in Electrical Engineering on measurement circuit design, device characterization and fabrication of scaled SONOS nonvolatile memories. He is a member of the IEEE Electron Devices Society (EDS) and the Sigma Xi research honorary.

Marvin H. White was born in the Bronx, New York on September 6, 1937. He received an A.S. degree in Engineering from the Henry Ford Community College (1957) a B.S.E. degree in Physics and Math (1960), M.S. degree in Physics (1961) from the University of Michigan and a Ph.D. degree in Electrical Engineering (1969) from the Ohio State University. In 1961 he joined the Westinghouse Solid-State Laboratory in Baltimore, MD. where he worked on advanced military and NASA imaging systems. From 1961 - 1981 he worked at Westinghouse as an Advisory Engineer in the design of low-power, custom integrated circuits with technologies of CMOS, Bipolar, MNOS and CCDs. During this period he was an adjunct Professor at the Electrical Engineering Depart-ment of the University of Maryland and a visiting Fulbright Professor at the Catholique Universite' de Louvain in Louvain-la-Neuve, Belgium.

In 1981, he became the Sherman Fairchild Professor in Solid-State Studies and Electrical Engineering at Lehigh University. At Lehigh he has developed a graduate program in microelectronics with research on SONOS nonvolatile memory devices, CMOS device modeling, studies of the Si-SiO_2 interface, SiC devices, and custom integrated circuits and sensors. He has graduated 23 Ph.D. students in microelectronics. He has served as a Visiting Researcher at the Naval Research Laboratories (1987) and a Program Director in Solid- State and Microstructures at the National Science Foundation (1995-96). In 1997 he received the Eleanor and Joseph Libsch Research Award at Lehigh University. He is currently the Director of the Sherman Fairchild Center for Solid-State Studies.

Prof. White is an IEEE Fellow (1974) and the recipient of the J. J. Ebers Award (1997) and the Masaru Ibuka IEEE Consumer Electronics Award (2000). In 1982 he was the IEEE Electron Devices Society (EDS) National Lecturer and is presently a Distinguished EDS Lecturer. He has served on IEEE/EDS committees, in particular, membership, and education. He is a member of Eta Kappa Nu and Sigma Xi.

FEATURING

A Device that Has Traveled in Outer Space

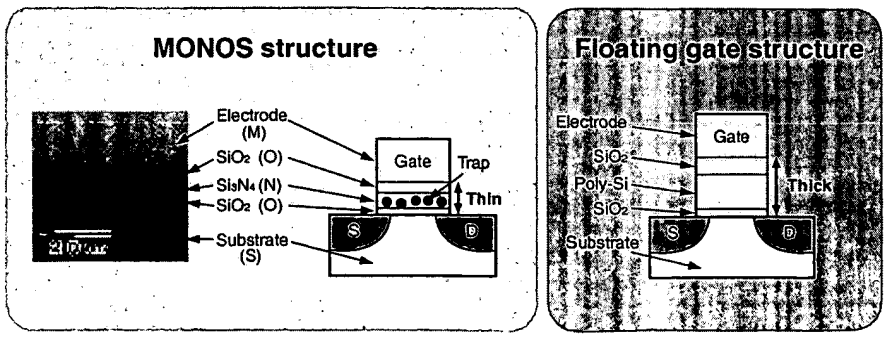
Low-Cost Embedded Nonvolatile Memory Device Technology: MONOS

- **High reliability**
  – Charge storage in a nitride film –
- **Narrow distribution of threshold voltages obviates the need for a "verify" operation to match distribution widths narrowly**
  – Makes circuit design easier –
- **Simple device structure makes chips easier to manufacture**
  – Expected to be usable through the 0.1 μm generation –
- **Low-cost embedded nonvolatile memory technology**
  – Low-voltage write and erase operations achieved by the use of hot carrier injection–

While MONOS (metal-oxide-nitride-oxide-semiconductor) is not a new nonvolatile memory technology, it has not received much attention until recently. The floating gate technology has remained as the mainstream nonvolatile memory technology, mostly due to the MONOS data retention characteristics being inferior. However, MONOS' reputation has begun to change over in recent years.

Figure 1 compares the MONOS and floating gate device structures. As can be seen in figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data. In the US, MONOS is used in satellites and spacecraft that wander for long periods between the planets. So why is it that MONOS, which is thought to have poor data retention characteristics, is used in the harsh environment of outer space, where they are constantly bombarded by high-energy particles? The reason lies in the structure and operating principles of the MONOS device. MONOS devices are actual highly stable and reliable devices.

Recently, the idea of storing 2 bits in a single memory transistor cell by using the features associated with storing charge on in the insulation layer in the MONOS device has been proposed. This makes it possible for MONOS to be the highest density nonvolatile memory technology, and has resulted in increasing interest in this technology. Another point is that the limits of the floating gate nonvolatile memory technology are now in sight, and MONOS is seen as having the potential to be the next generation nonvolatile memory technology. Sony's researchers already see how MONOS can be adapted for use through the 0.1 μm feature size generation. Furthermore, Sony is now developing MONOS as a key technology for product differentiation in Sony's system-on-chip (SoC) business.



■ Figure 1 MONOS and Floating Gate Structures Comparison

MONOS Device Structure and Operating Principles

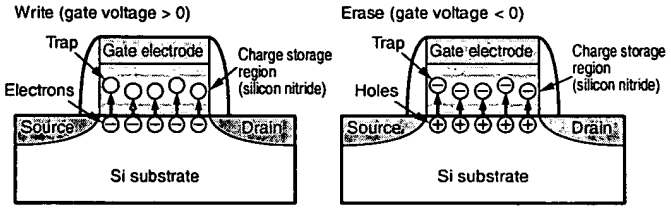
As shown in figure 1, the MONOS structure consists of ONO film layers (oxide-nitride-oxide) between the substrate and the gate. While the nitride film in the center of the ONO film layers is an insulator, there are large numbers of traps located in that layer and it can capture and store charge. This layer can be made to function as a charge storing means by injecting and rejecting charge from these traps.

There are two techniques for injecting and rejecting charge. One is a write and erase method in which electrons are injected or rejected with tunnel current technique over the whole area under the gate electrode as shown in figure 2. The other method uses hot carriers as shown in figure 3. The tunnel current technique achieves a larger number of write/erase cycles and assures high reliability. In contrast, the hot carrier method allows lower write and erase operating voltages to be used and achieves higher speeds. Lowering the operating voltage also leads to reduced manufacturing costs, and is effective for one-time programming (OTP) and multi-time programming (MTP) products. Recently, the idea of MONOS devices that store 2 bits in a single memory transistor cell using this principle has proposed. These are called NROM devices.

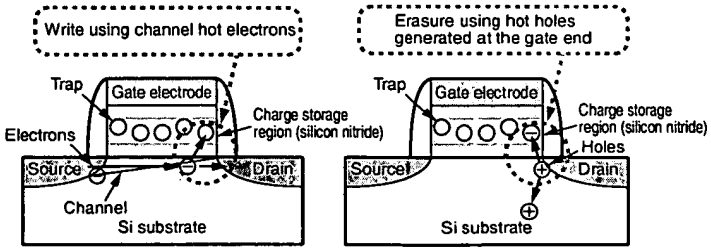
High Reliability

MONOS' main advantage lies in its stability and durability. As shown in figure 4, there is almost little charge leakage in MONOS devices even if there are defects in the extremely thin oxide film between the nitride layer that stores the charge and the substrate. This is because charge is stored in an insulating film layer. In contrast, in the floating gate type device, all stored charge is lost if a defect is created at even one location. This is like the shipbuilding technique in which large numbers of isolated chambers are used. If a defect is opened in one, the area that is flooded is limited to that chamber. That is, even if a defect is created between the substrate and the layer (nitride film) that stores the charge, it is impossible for all the charge stored in the insulating film to escape through that defect. In contrast, conventional floating gate ships (devices) would flood and sink immediately if even one defect appeared. This is because the floating gate, which stores the charge, is itself a conductor. This MONOS durability is the reason MONOS is used in outer space, where devices are constantly bombarded by high-energy particles.

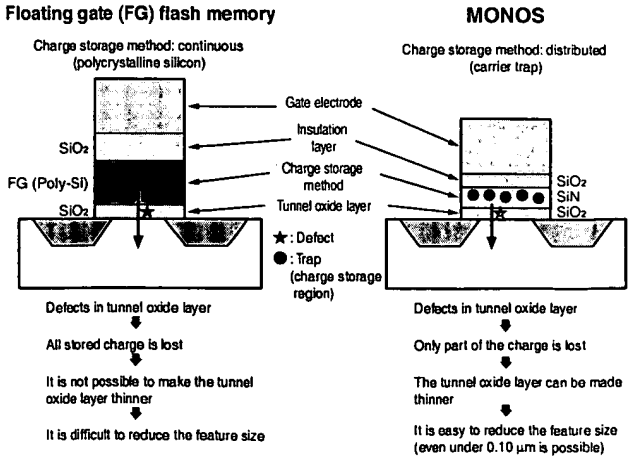
MONOS has another advantage. That advantage is that it leaks. It cannot be denied that this is the reason that MONOS is not widely used. However, as our study of the MONOS structure has progressed, and we have had more experience using MONOS, we have come to realize the following. There is no sample-to-sample variation in the amount of leakage in MONOS devices. That is, all boats (devices) leak water at the same rate. This means that it is possible to predict when to get off the boat in safety. That is, these boats are actually much safer than boats that appear solid but may actually rupture and sink at any time.



■ **Figure 2 MONOS Write and Erase Operations Using F-N Tunnel Current Injection Technique Conceptual Overview**



■ **Figure 3 MONOS Write and Erase Operations Using Hot Carriers Injection Technique Conceptual Overview**



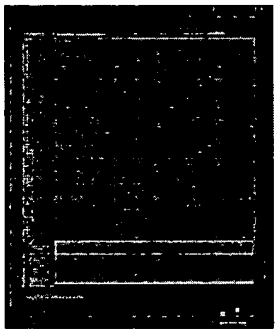
■ **Figure 4 MONOS Features: Charge Does not Escape even with Defects in the Oxide Layer**

Narrow Threshold Voltage Distribution Obviates the Need for Operations to Narrow the Distribution

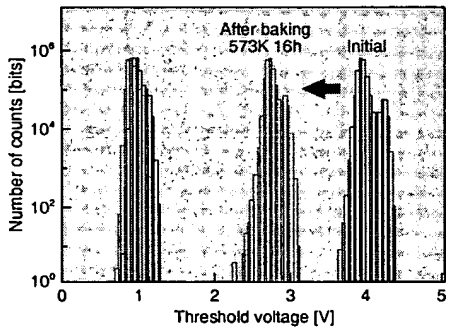
Sony has taken the lead in this area by creating the 4 Mbit MONOS test memory chip shown in figure 5. (This device was announced at the 2001 IEDM conference.) Figure 6 shows the accelerated test results for the written threshold voltage distribution retention characteristics. Although the threshold voltage falls, the distribution does not break. Furthermore, as shown in table 1, the width of the distribution itself is narrower, being only 1/3 that of the conventional floating gate device, and thus is extremely well matched. Also, the threshold voltage distribution does not break after repeated write and erase cycles. Figure 7(a) shows the change in the width of the distribution with writing, and figure 7(b) shows that change with erasure. As you can see, the width of the distribution does not change with these processes. Even with repeated write and erase cycles, the distribution remains narrow. (See figure 8.) This is one of MONOS' superior characteristics, and is a significant advantage when designing memory circuits. In the conventional floating gate device, the threshold voltage distribution must be narrowed with an operation called "verify" during write and erase. This is a difficult circuit operation and complicates circuit design. The MONOS structure may be able to obviate the need for this "verify" operation.

Device with a Simple Ease to Fabricate Structure

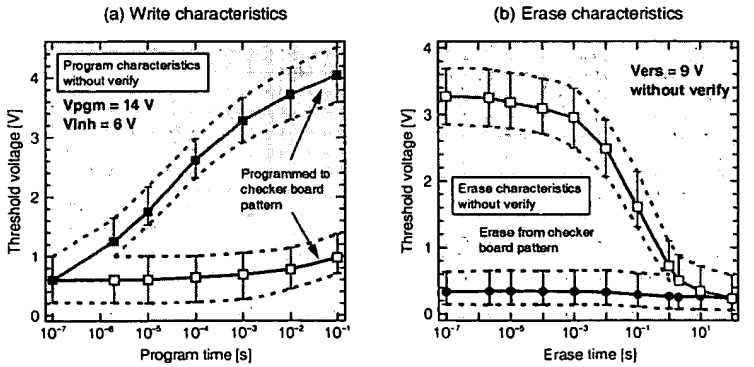
Another significant feature of the MONOS structure is the simplicity of that structure. Figure 9 shows the cross section of a MONOS device imaged with a transmission electron microscope (TEM). At first look, it appears to be identical to an ordinary MOS transistor. Sony already sees the way to use this structure in 0.1 μm generation devices. The simplicity of this structure is also extremely important for embedding these devices in larger chips. This is because the simpler the structure the fewer the additional fabrication steps required for embedding. If only MONOS transistors are added, only 2 or 3 mask steps need to be added. Normally, embedding other types of flash memory requires an additional 6 or 7 masks. This is because these other devices require that the high-voltage transistors that handle the high voltages required for write and erase operations must be created separately.



■ **Figure 5 4 Mbit MONOS Test Chip**



■ **Figure 6 4 Mbit MONOS Test Chip Memory Retention Characteristics**



■ **Figure 7 Write and Erase Characteristics of MONOS Threshold Voltage Distribution**

■ **Table 1 MONOS and Floating Gate Threshold Voltage Distributions Comparison**

	MONOS	Floating gate devices		
	This product	ref.1	ref.2	ref.3
Write state	0.057	0.165		
Erase state	0.058	0.15		0.15

Standard deviation (V)

Standard deviation in MONOS is about 1/3

[1] K.Yoshikawa, et al., IEDM92, p.595 (1992).
[2] R.Shirota, NVSMW 2000, p.22 (2000).
[3] P.L.Rolandi, et al., NVSMW 2000, p.75 (2000).

Low-Cost Embedded Nonvolatile Memory Technology

If nonvolatile memory could be embedded with only the addition of 2 or 3 masks, that is, with only a cost increase of about 10% over that of the original chip, we could expect a large demand for OTP and MTP applications. Another way of looking at this would be that low-cost embedded nonvolatile memory technology would function as a product differentiation technology. Specific examples that would be possible include inclusion of embedded nonvolatile memory in the camera processor IC that forms, along with the CMOS image sensor, a camera module, in a GPS module that fits in a Memory Stick slot, or in a camera module interface chip. (See figure 10.)

Other applications where this would be useful include the programmable impedance matching circuit used in high-precision D/A converters and high-precision power supplies and the recording of data used for chip authentication.

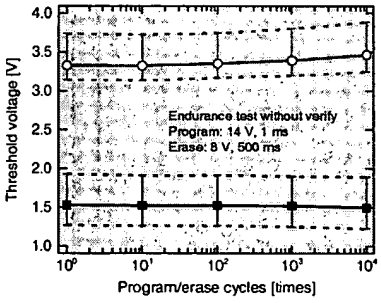
Sony is now studying the possibility of reducing the MONOS write and erase voltages to realize low-cost embedded nonvolatile memory technology using only 2 or 3 additional masks. Sony is attempting to reduce the voltages required by switching from the use of F-N tunnel current, which requires 12 to 14 V for write and erase, to a technique that uses hot carriers. Figure 11(a) shows the write characteristics when channel hot electrons are used, and figure 11(b) shows the erase characteristics using hot hole injection. With absolute voltages around 5 to 6 V, these techniques can achieve fully adequate write and erase operations.

Future Developments

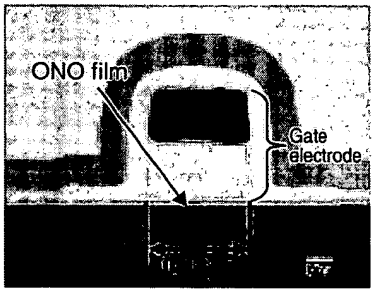
Sony is making progress on embedding MONOS nonvolatile memory in a 0.18 μm CMOS process. We are working on creating new applications and expect to release products using this technology during 2003.

This one process is not the only process that requires embedded nonvolatile memory. To take maximum advantage of this newly-developed technology, Sony plans to apply it in as many processes as possible. We think that MONOS' stability and durability will make this easy.

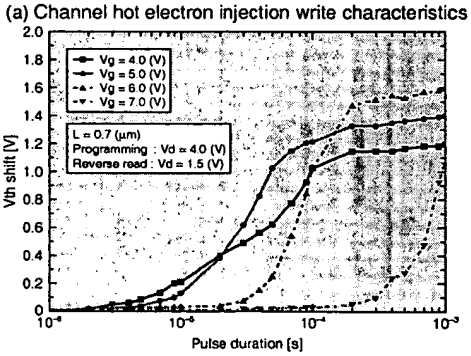
Keep your eye on Sony's low-cost nonvolatile memory technology.



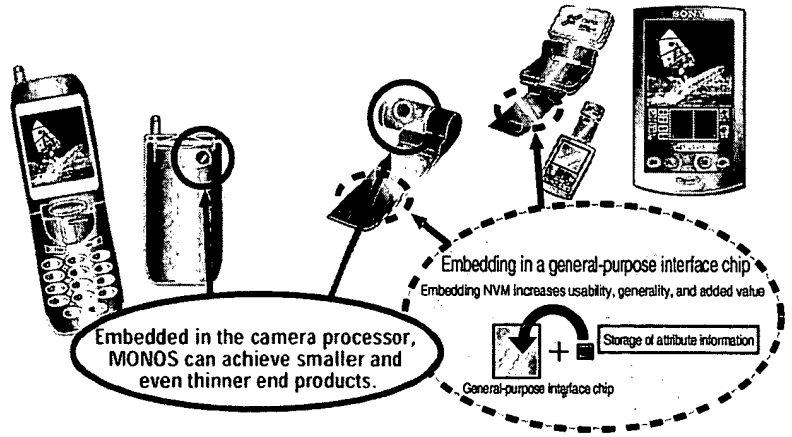
■ **Figure 8 4 Mbit MONOS Test Chip Endurance Characteristics**



■ **Figure 9 TEM Photograph for MONOS Memory Transistor**



■ **Figure 11 Characteristics of the Embedded Low-Voltage MONOS Memory Cell**



■ **Figure 10 Embedded MONOS Applications**